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IN THE CLAIMS:

1. (Currently Amended) A mechanism for resource allocation in a processor, comprising:

categorization logic, associated with an earlier pipeline stage, that generates instruction type information for instructions to be executed in said processor;

queuing logic, in which said instructions and said instruction type information are stored in an order based on a priority of said instructions derived from a priority of functional units in said processor; and

priority logic, associated with a later pipeline stage, that allocates functional units of said processor to execution of said instructions in said order based on said instruction type information.

2. (Original) The mechanism as recited in Claim 1 wherein said categorization logic causes said instruction type information to be stored and tagged in a queue containing said instructions.

3. (Original) The mechanism as recited in Claim 1 wherein said earlier pipeline stage is a fetch/decode stage of said processor.

4. (Original) The mechanism as recited in Claim 1 wherein said instructions are ungrouped when said categorization logic generates said instruction type information.

5. (Original) The mechanism as recited in Claim 1 wherein said instruction type information defines at least four categories of instruction.